**ABSTRACT OF THE DISCLOSURE**

A PLL clock generator generates an output signal with a frequency N times (where $N \geqq 1$) as high as that of an input signal. The clock generator includes: a frequency divider for dividing the frequency of a clock signal by N so as to output a frequency-divided clock signal; a phase comparator for detecting a phase difference between the input signal and the output signal of the frequency divider so as to output a phase difference signal including information representing the phase difference; a LPF for smoothing the phase difference signal; a VCO for generating the clock signal, of which the frequency is determined by the output of the LPF, and outputting the clock signal to the frequency divider; and a phase shifter for shifting the phase of the output signal of the frequency divider in accordance with the phase difference signal.